CN3927ELC

Enhanced Low Cost Voice Coil Motor Driver IC with I²C Interface

Description

The CN3927ELC is single 10-bit DAC with 120mA output current sinking capability. Designed for linear control of voice coil motors, the CN3927ELC is capable of operating voltage from 2.3V to 5.5V. The SAC (Smart Actuator Control) mode is applied to minimize mechanical vibrations automatically. The SAC mode highly improves the actuator's settling time and tolerance coverage compared with conventional LSC (Linear Slope Control) mode. The DAC is controlled via a I²C serial interface that operates DAC by clock rates up to 400kHz.

The CN3927ELC incorporates an internal Power-UP Reset (POR) and power down features using external XSD pin or internal PD bit that reduces the current consumption of the device to be less than 1uA .

The CN3927ELC is designed for auto focus and optical zoom camera phones, digital still cameras, and camcorders applications. The I²C address for the CN3927ELC is 0x18.

Features

- WLCSP package for minimum footprint
- Fast Settling Mode (SAC/EDLC)
- 10-bit D-to-A converter
- Current sinking of 120mA (default)
- Current sinking of 150mA (Option)
- 117μA Iout resolution
- NRC Control Mode
- Fast I²C serial interface (1.8V input available)
- Low current SLEEP/XSD mode
- 2.3 to 5.5 V power supply

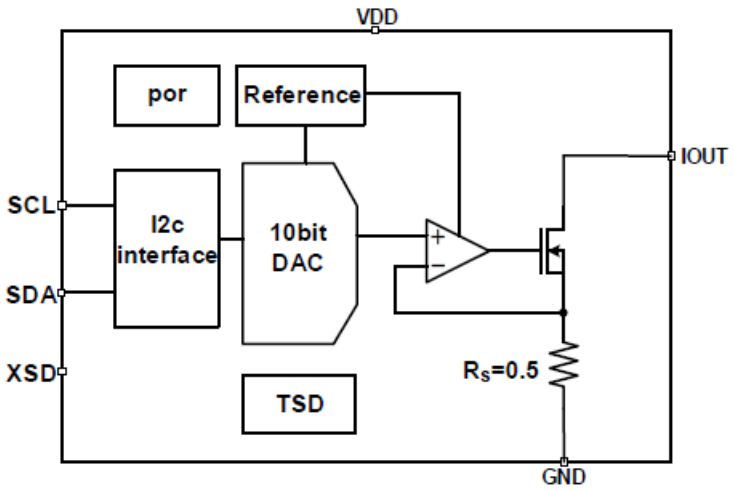
Applications

- Digital camera
- Cell phone
- Lens auto focus

Package

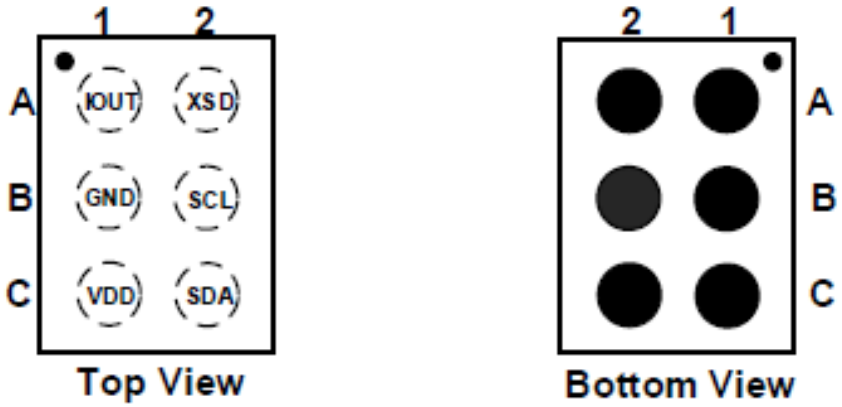
- 6-Bump Chip Scale Package
- 0.57mm(W) x0.97mm(H) x 0.28mm(T)
- 0.4mm Bump Pitch

Block Diagram



1. Pin Information

◆ Pin Assignments



◆ Pin Description

Pin Name	Pin Number	Description
IOUT	A1	Output current Sink
XSD	A2	Shutdown mode (active low)
GND	B1	Ground
SCL	B2	I^2C data
VDD	C1	Power Supply
SDA	C2	I^2C clock

2. Ordering Information

Order Part Number	Top Marking	Pb-Free	T_A	Package	
CN3927ELC	27E	Yes	-40 to +85°C	WLCSP6	Tape Reel,3K

3. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maxim rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Min.	Max.	Unit
VDD	Supply Voltage Range		6.5	V

Vin	Logic Input Voltage Range	-0.3	Vdd+0.3	V
T_J	Junction Temperature		150	°C
T_S	Storage Temperature Range	-40	150	°C
	Operating Temperature Range	-40	85	°C
ESD rating	Human Body Model (HBM)	6		KV

4. Recommend Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Input Voltage	2.3	2.8	5.5	V
Vin	Control Input Voltage	0		VDD	V
SCL	I2C Bus Clock Rate			400	KHz
	Junction Temperature Range	-40		125	V
	Ambient Temperature Range	-40		85	°C

The Recommended Operating Conditions table defines the conditions for actual device operation to ensure optimal performance to the datasheet specifications. CHIPNEXT does not recommend exceeding them or designing to Absolute Maximum Ratings.

5. Electrical Characteristics

T_A = 25°C, VDD =2.8V, V_{IN}=1.8V (unless otherwise specified)

Characteristics	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max	Units
Operation current						
Supply Voltage	V_{DD}	Linear mode	2.3	2.8	5.5	V
Supply Current	I_Q	Quiescent mode(DAC=0)		0.3		mA
	I_{ACT}	Operation mode (DAC ≠ 0)			1	mA
	I_{SD}	Shutdown mode(XSD=0)	-1		1	uA
	I_{PD}	Power down mode(PD=1)	-1		1	uA
Wait time	t_{OPR}	After VDD rising	1			ms
Logic Input/Output(XSD)						
Input current			-1		1	uA
Low level input voltage	V_{IL}	VDD=2.8V			0.4	V
High level input voltage	V_{IH}	VDD=2.8V	1.2			V
D/A						
Resolution (1)		Target=117uA/LSB		10		bit
Relative Accuracy (1) (2)	INL	Code from 1 to 1023	-4		+4	LSB

Differential Nonlinearity (1) (2)	DNL	Guaranteed Monotonic	-1		+1	LSB
Max output current	Imax	Code=1023	116	120	124	mA
Output Driver						
Output Rdson	Rds	Rsense+Rsink, Iout=100mA, VDD=3V		2.0		Ω
Output Current @ PD			-1		1	uA
Logic Input and Output (SCL,SDA)						
Input Current			-1		1	uA
Low level Input Voltage	V_{IL}				0.54	V
High level Input Voltage	V_{IH}		1.26			V
SDA low level Input Voltage (open drain)	V_{IH}	Sink current =3mA			0.4	V
Glitch rejection			50			ns

(1) These are guaranteed by design spec

(2) Linearity is guaranteed for code 32 through code 992

6. I2C Protocol

6.1 Start and Stop Condition

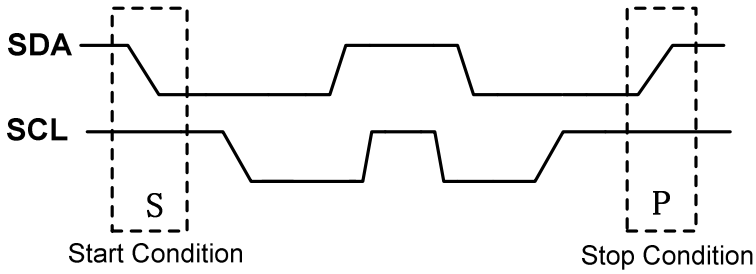


Figure 1. I2C Start and Stop Condition

Within the procedure of the I2C-bus, unique situations arise which are defined as START(S) and STOP(P) conditions. A HIGH to LOW transition on the SDA line while SCL is HIGH is one of such unique cases. This situation indicates a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition.

6.2 I^2C Data Transfer

10.3 Actuator Fast Settling Control

Mechanical ringing is an inherent problem in VCM. Various fast settling algorithms are implemented for reducing mechanical ringing and achieving very fast settling time, and as a result, enhances autofocus response times, image quality, and user experience. These algorithms incorporate a wide band of tolerance around the vibration period of the VCM to compensate for manufacturing variability in the mechanical vibration period (t_{VIB}) of VCM.

CN3927ELC offers various fast settling modes which are trade-off between operation time and tolerance. User can choose optimal fast settling mode for each application.

■ **Operation Time and Tolerance for Different Modes**

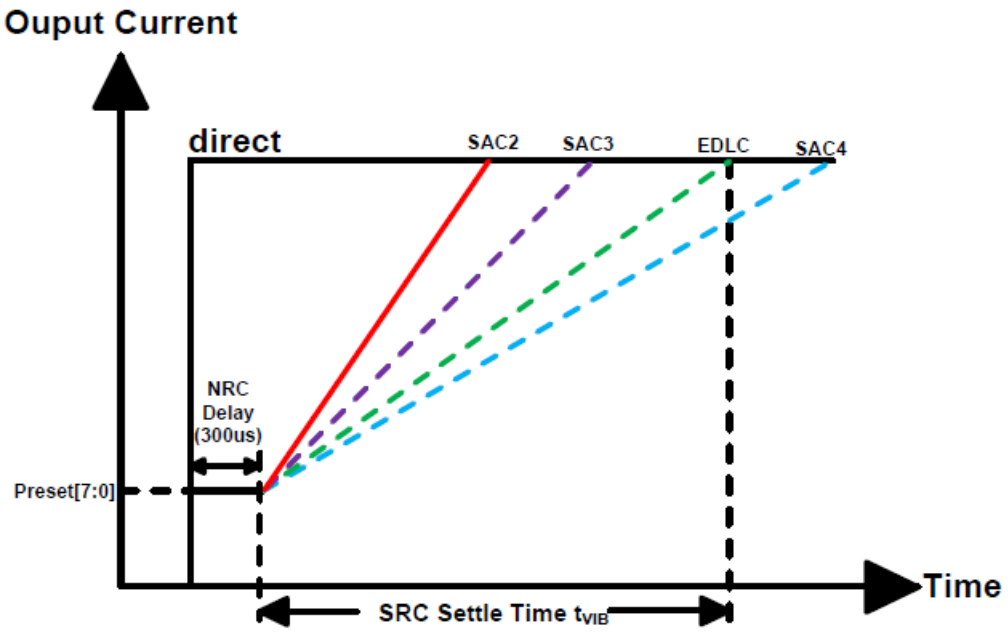


Figure 11. SAC Setting Time

Mode	Operation time(1)	Tolerance of VCM(2)
Direct	-	-
SAC2	0.50 x t_{VIB}	±9%
SAC3	0.75 x t_{VIB}	±16%
EDLC	1.00 x t_{VIB}	±24%
SAC4	1.25 x t_{VIB}	±37%

(1) The time to reach a target current.

(2) Tolerance can be changed by mechanical characteristics of specific actuators.

■ **Test Results for Different Modes**

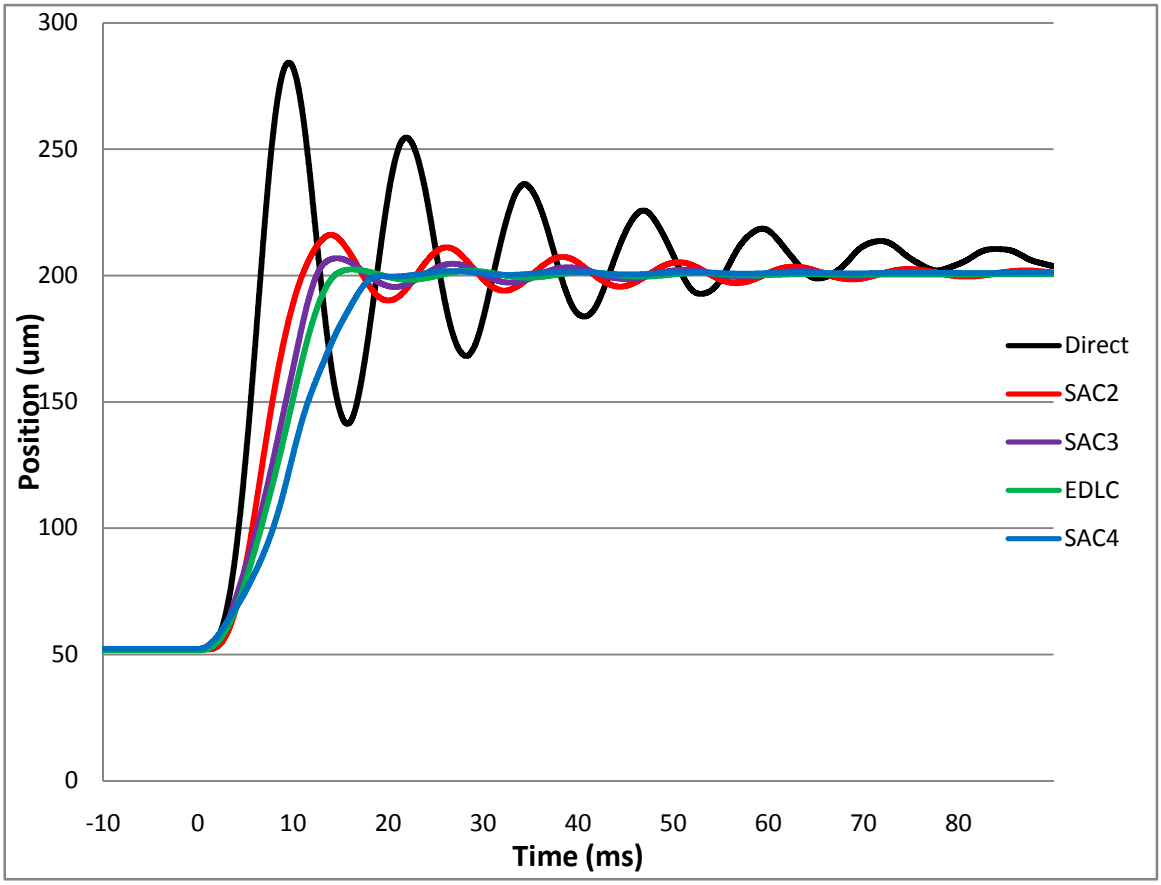


Figure 12. Test Results for Different Advanced Fast Settling Mode

10.4 Noise Reduction Control (NRC) Mode

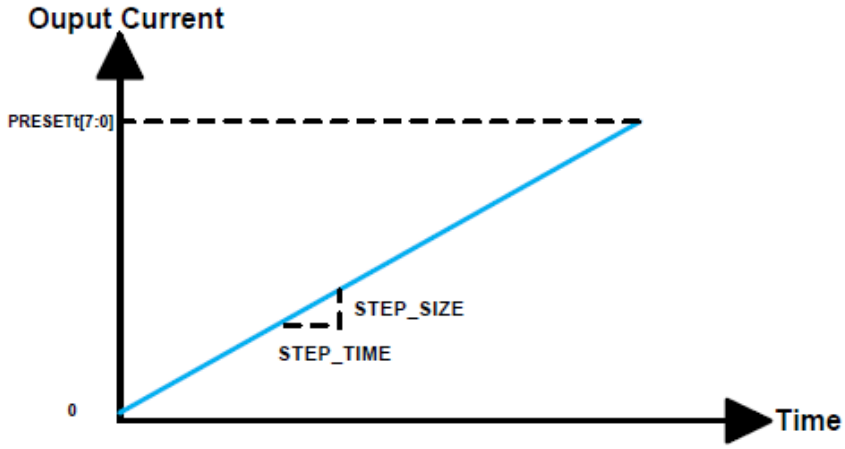


Figure 13. NRC Start

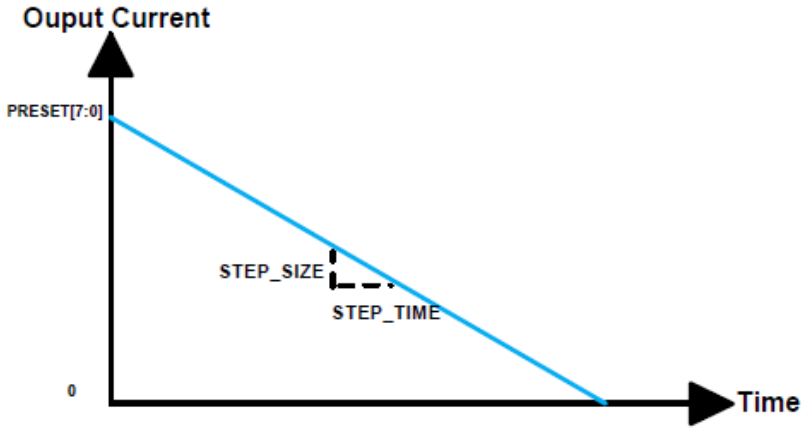


Figure 14. NRC Landing

※ The NRC start and NRC landing are modes reducing sound noise level from the used VCM application.
※ The NRC start and NRC landing algorithm is set by PRESET[7:0] ,STEPTIME and NRC_STEP[1:0].
※ PRESET[7:0] is NRC current setting.
※ NRC_STEP{[1:0] is NRC Step Size, while STEPTIME[7:0] controls the time for each step

11. Typical Application Circuit

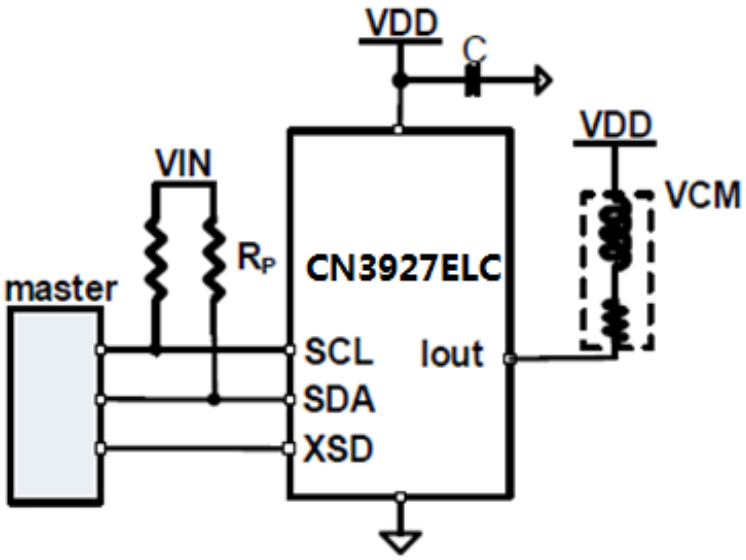


Figure 15. Typical Application Circuit

※ Power supply decoupling capacitor (C) should be placed as close to the VDD and VSS as possible.
※ The value of C is recommended more than 1uF.
※ PCB pattern of VDD, GND, OUTP and OUTN should be as short and wide as possible.

12. WLCSP-6 Package of Outline (0.20mm partial ball size/0.40mm ball pitch)

(All Units of Measure = mm)