# CN3938V : High Drive Bi-directional Voice Coil Motor Driver IC with I2C interface

## 1. Description

The CN3938V is single 10-bit DAC with ± 130mA output current source/sink capability. Designed for bi-directional linear control of voice coil motors, the CN3938V is capable of operating voltage from 2.3V to 5.5V. The DAC is controlled via a I2C serial interface that operates DAC by clock rates up to 1000kHz.

The CN3938V incorporates with a UVLO reset circuit, power-down function, and exactly matched sense resistor. UVLO reset circuit ensure when supply power up, DAC output is to 0V until valid write-bit value takes place. It has a power down features that reduces the current consumption of the device to 1uA maximum.

The CN3938V is designed for auto focus and optical zoom camera phones, digital still cameras, and camcorders applications. The I2C Write/Read address for the CN3938V is 0x18/0x19 respectively.

## Features

- WLCSP package for minimum footprint
- Advanced SRC mode
- 10-bit D-to-A converter
- Current souring/sinking of ±130mA
- 194μA *Iout* resolution for ±100mA
- Fast I2C serial interface (1.8V input available)
- Low current sleep mode
- 2.3 to 5.5 V power supply

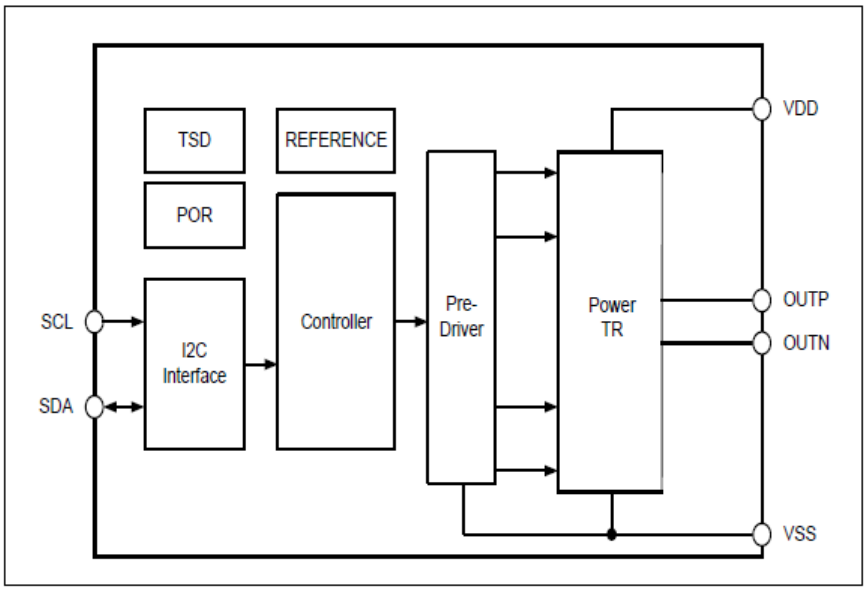
## Applications

- Digital camera
- Cell phone
- Lens auto focus
- Web camera

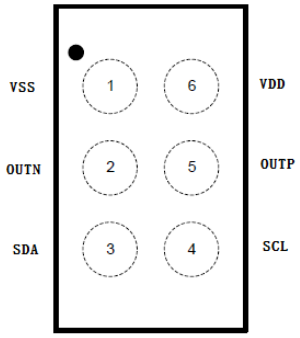
## Package

- 6-Bump Chip Scale Package
- 0.700mm(W) x1.100mm(H) x 0.280mm(T)
- 0.4mm Bump Pitch

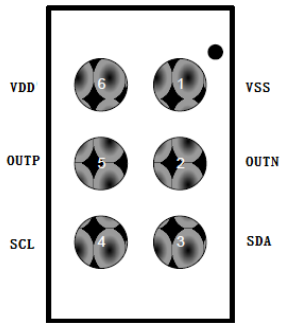
## 2. Functional Block Diagram



## 3. Pin Assignments




Top Side View




Bottom View

## 4. Pin Description

| Pin Name | Pin Number | Description |
|---|---|---|
| VSS | 1 | Ground |
| OUTN | 2 | I/O, H-bridge Output |
| SDA | 3 | $I^2C$ data |
| SCL | 4 | $I^2C$ clock |
| OUTP | 5 | I/O, H-bridge Output |
| VDD | 6 | Power Supply |

## 5. Ordering Information

| Order Part Number | Top Marking | Pb-Free | $T_A$ | Package |
|---|---|---|---|---|
| CN3938V | 38V | Yes | -40 to +85°C | WLCSP6 |

## 6. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maxim rating conditions for extended periods may affect device reliability.

| Parameter | | Conditions | Min. | Typ | Max. | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage | VDD | | | | 6.5 | V |
| Logic Input Voltage Range | Vin | | -0.3 | | VDD+0.3 | V |
| Junction Temperature | Tj | | | | 150 | °C |
| Storage Temperature Range | Ts | | -40 | | 150 | °C |
| Operating Temperature Range | | | -40 | | 85 | °C |
| ESD (HBM) | | | | 8 | | KV |

## 7. Recommend Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation to ensure optimal performance to the datasheet specifications. CHIPNEXT does not recommend exceeding them or designing to Absolute Maximum Ratings.

| Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| VDD, Supply Input Voltage | 2.3 | 3 | 5.5 | V |
| Vin, Control Input Voltage | 0 | | VDD | V |
| SCL, I2C Bus Clock Rate | | | 400 | KHz |
| Junction Temperature Range | -40 | | 125 | V |
| Ambient Temperature Range | -40 | | 85 | °C |

## 8. Electrical Characteristics

$T_A$ = 25°C, VDD=2.8V (unless otherwise specified)

| Characteristics | Symbol | Test Conditions | Limits | | | |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max | Units |
| **Overall** | | | | | | |
| Supply Voltage | VDD | | 2.3 | 2.8 | 5.5 | V |
| Supply Current | Ivdd | Quiescent mode (DAC≠512) | | 0.35 | | mA |
| | | Power Down Mode , | -1 | | 1 | uA |
| UVLO VDD threshold | Vth_uvlo | Iout<1uA, when VDD decrease to Vth_uvlo | | 2 | | V |
| UVLO hysteresis | Vhys_uvlo | | | 100 | | mV |
| Thermal shutdown Temp | Tjtsd | | | 145 | | °C |
| Thermal shutdown hys | Thys | | | 15 | | °C |
| **D/A & Driver** | | | | | | |
| Resolution | | Target=195uA/LSB | | 10 | | Bit |
| Positive Relative Accuracy | P_INL(1) | Code from 512 to 1023 | -4 | + | +4 | LSB |
| Positive Differential Nonlinearity | P_DNL(1) | Guaranteed Monotonic | -1 | | 1 | LSB |
| Negative Relative Accuracy | N_INL(1) | Code from 0 to 512 | -4 | + | +4 | LSB |
| Negatives Differential Nonlinearity | N_DNL(1) | Guaranteed Monotonic | -1 | | 1 | LSB |
| Zero Code Error (2) | ZCE | DAC=Zero Current Code=512 | -0.01 | | 0.01 | mA |
| Max output current | Imax | Code=0/1023 | +/-126 | +/-130 | +/-134 | mA |
| Output Rds on | Rds | Rsense+Rsink, Iout=60mA, | | 2.5 | | ohm |
| Output current @ Power Down | Iout | | -0.1 | | +0.1 | uA |
| **Logic Input / Output (SCL,SDA)** | | | | | | |
| Logic input (SDA, SCL) low level | $V_{IL}$ | | | | 0.54 | V |
| Logic input (SDA, SCL) high level | $V_{IH}$ | | 1.26 | | | V |
| Logic input current | $I_{IN}$ | Vin from 0V to VDD | -1 | | 1 | uA |
| Output voltage (SDA) | Vol | Iload=3.0mA | | | 0.10 | V |
| Hardware Reset Detection time(1) | $T_{HRST}$ | SCL& SDA=3mA | | | 3 | ms |
| Setup time for normal operation(1) | $T_{OPR}$ | | 100 | | | us |

(1) These are guaranteed by design and characterization

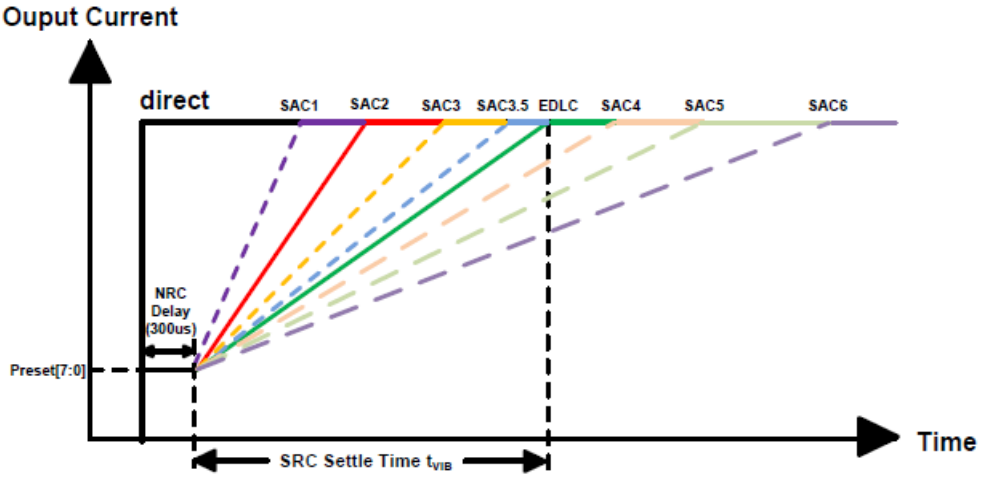
(2) Zero current code =512 (default)

## 11. Slew Rate Control (SRC) Setup Method

Mechanical ringing is an inherent problem in VCM. Various fast settling algorithms are implemented for reducing mechanical ringing and achieving very fast settling time, and as a result, enhances autofocus response times, image quality, and user experience. These algorithms incorporate a wide band of tolerance around the vibration period of the VCM to compensate for manufacturing variability in the mechanical vibration period ($t_{VIB}$) of VCM.

CN3938V offers various fast settling modes which are trade-off between operation time and tolerance. User can choose optimal fast settling mode for each application.

### ■ Operation Time and Tolerance for Different Modes




***SRC Setting Time***

| SRC Mode | Operation time(1) | Tolerance of VCM(2) |
|---|---|---|
| Direct | - | - |
| EDLC | 1.00 x $t_{VIB}$ | ±18% |
| SAC1 | 0.33 x $t_{VIB}$ | ±8% |
| SAC2 | 0.50 x $t_{VIB}$ | ±9% |
| SAC2.5 | 0.67 x $t_{VIB}$ | ±15% |
| SAC3 | 0.75 x $t_{VIB}$ | ±16% |
| SAC3.5 | 0.96 x $t_{VIB}$ | ±24% |
| SAC4 | 1.25 x $t_{VIB}$ | ±37% |
| SAC5 | 1.71 x $t_{VIB}$ | ±43% |
| SAC6 | 1.96 x $t_{VIB}$ | ±63% |

(1) The time to reach a target current.

(2) Tolerance can be changed by mechanical characteristics of specific actuators.

■ **Test Results for Different SRC Modes**

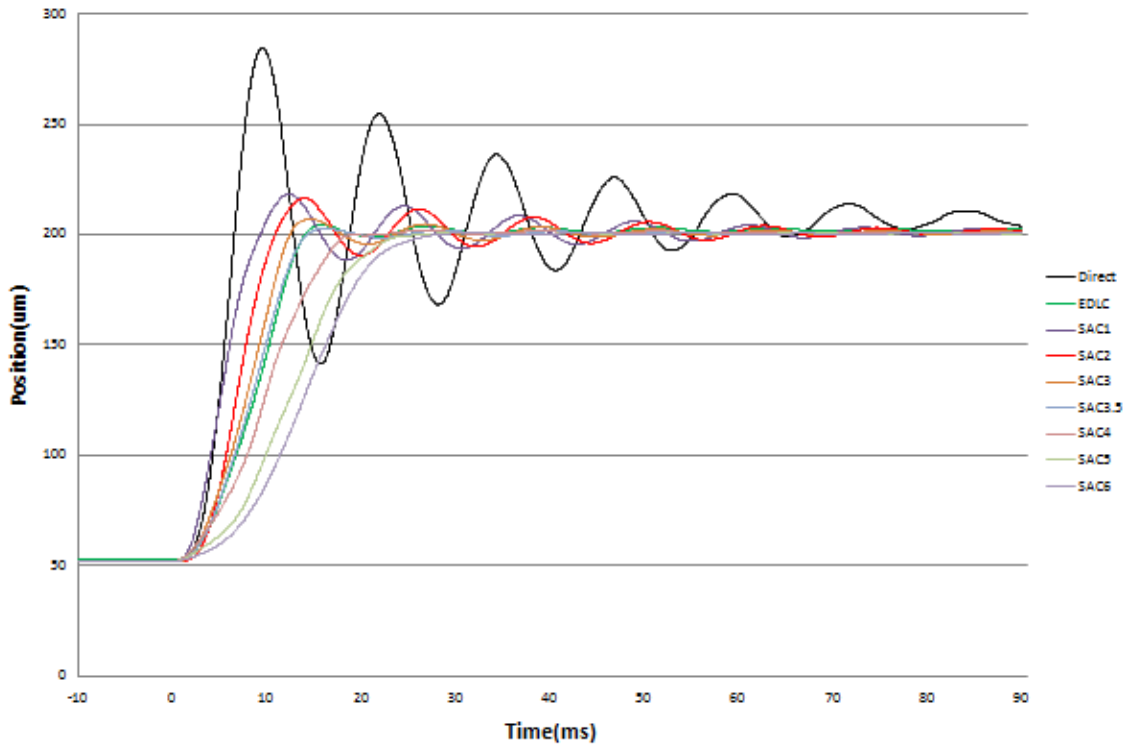
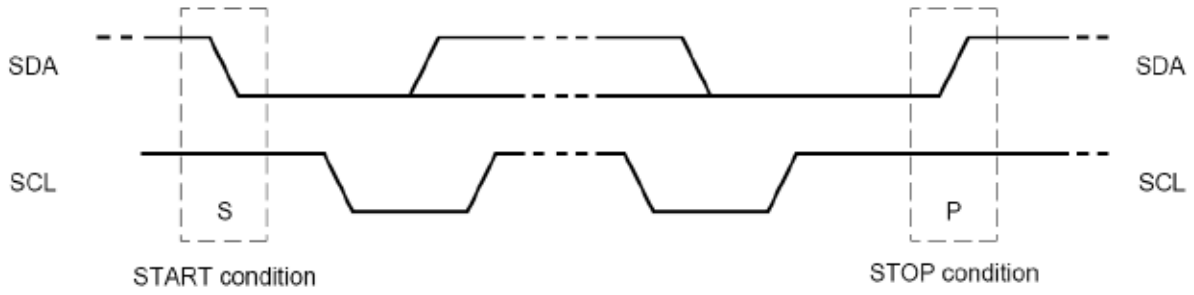



*Figure 8. Test Results for Different Advanced SRC Mode*

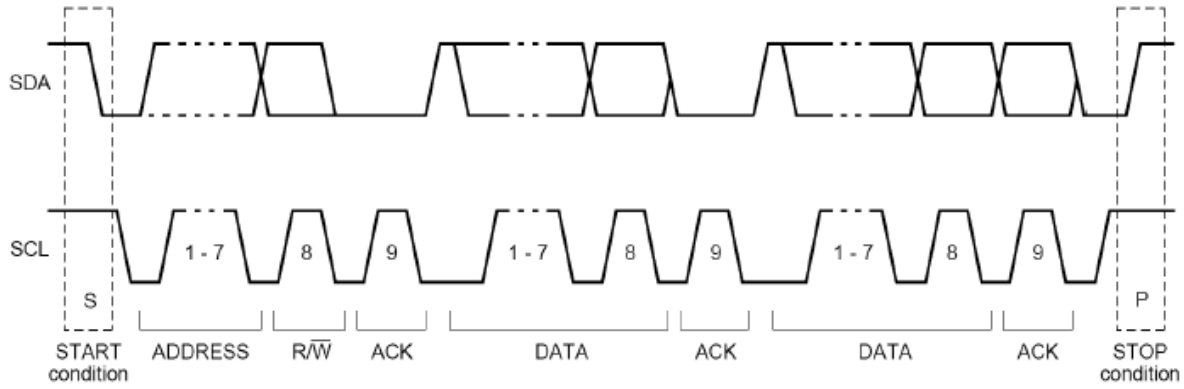
## 12. I2C Protocol

### 12.1 Start and Stop Condition:




Within the procedure of the I2C-bus, unique situations arise which are defined as START(S) and STOP(P) conditions. A HIGH to LOW transition on the SDA line while SCL is HIGH is one of such unique cases. This situation indicates a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition.

### 12.2 Complete I2C Data Transfer:




Data transfers follow the above format. After the START condition(S), a slave address is sent. A data transfer is always terminated by a STOP condition(P) generated by the master. However, if the master still needs to communicate on the bus, it can generate a repeated data transfer.

## 12.3 I2C Timing:

| Parameter | Symbol | Fast-mode | | Fast-mode Plus | | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| Serial clock frequency | $f_{SCL}$ | | 400 | | 1000 | kHz |
| Hold time (repeated) START condition. | $t_{HD;STA}$ | 0.6 | - | 0.26 | - | us |
| Low period of the SCL clock | $t_{LOW}$ | 1.3 | - | 0.5 | - | us |
| High period of the SCL clock | $t_{HIGH}$ | 0.6 | - | 0.26 | - | us |
| Set-up time for a repeated START condition | $t_{SU;STA}$ | 0.6 | - | 0.26 | - | us |
| Data hold time | $t_{HD;DAT}$(1) | 0 | - | 0 | - | us |
| Data set-up time | $t_{SU;DAT}$ | 100 | - | 50 | - | ns |
| Rise time of both SDA and SCL signals | $t_r$ | $20+0.1C_b$(2) | 300 | $20+0.1C_b$(2) | 120 | ns |
| Fall time of both SDA and SCL signals | $t_f$ | $20+0.1C_b$(2) | 300 | $20+0.1C_b$(2) | 120 | ns |
| Set-up time for STOP condition | $t_{SU;STO}$ | 0.6 | - | 0.26 | - | us |
| Bus free time between a STOP and START condition | $t_{BUF}$ | 1.3 | - | 0.5 | - | us |
| Capacitive load for each bus line | $C_b$ | - | 400 | - | 550 | pF |
| Pulse width of spike suppress | $t_{SP}$ | 0 | 50 | 0 | 50 | ns |
| Data valid time(3) | $t_{VD;DAT}$ | - | 0.9 | - | 0.45 | us |
| Data valid acknowledge time(4) | $t_{VD;ACK}$ | - | 0.9 | - | 0.45 | us |
| Noise margin at the LOW level | $V_{nL}$ | $0.1V_{DD}$ | - | $0.1V_{DD}$ | | V |
| Noise margin at the HIGH level | $V_{nH}$ | $0.2V_{DD}$ | - | $0.2V_{DD}$ | | V |

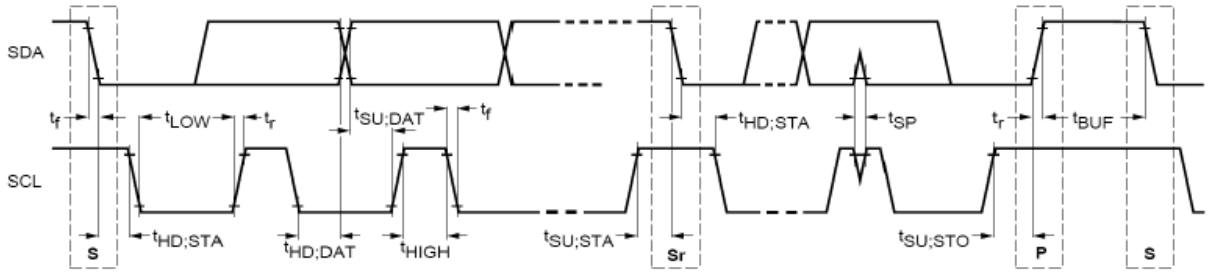
(1) A master device must provide a hold time of at least 100ns for the SDA signal to bridge the undefined region of the falling edge of SCL. The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period ($t_{LOW}$) of the SCL signal.

(2) Cb is the total capacitance of one bus line in pF, tr and tf are measured between 0.3VDD and 0.7VDD.

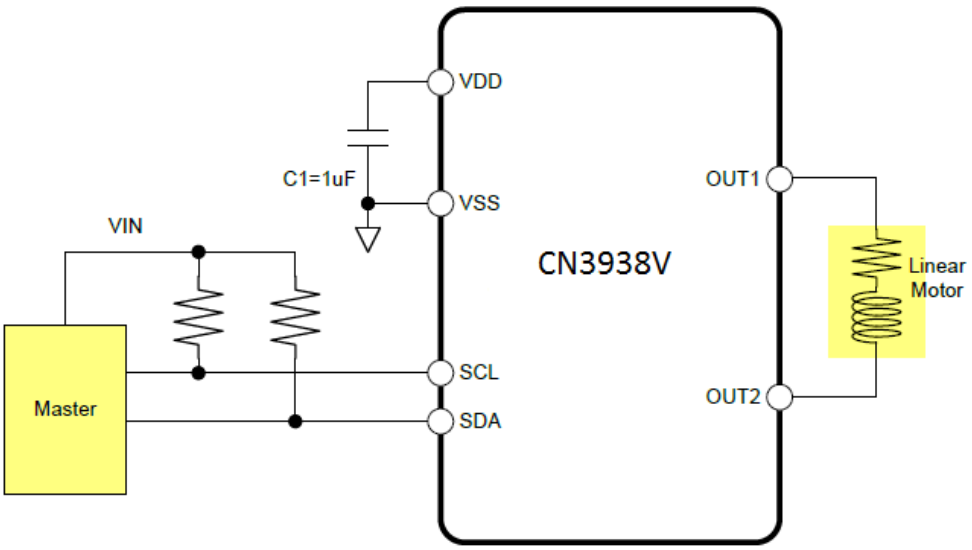
(3) $t_{VD;DAT}$ = time for data signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is

worse).

(4) $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).




## 13. Typical Application Circuit




※ Power supply decoupling capacitor (C1) should be placed as close to the VDD and VSS as possible.

※ The value of C1 is recommended more than 1uF.

※ PCB pattern of VDD, GND, OUTP and OUTN should be as short and wide as possible.

## 14. WLCSP 6 Package of Outline (All Units of Measure=mm)