CN3969P
# Voice Coil Motor Driver IC with 10KByte EEPROM

Description

The CN3969P is a single 10-bit DAC with 120mA output current sinking capability and has an 10KByte EEPROM Memory. Designed for linear control of voice coil motors, the CN3969P is capable of operating voltage from 2.3V to 3.6V. The SAC (Smart Actuator Control) mode is applied to minimize mechanical vibrations automatically. The SAC mode highly improves the actuator's settling time and tolerance coverage compared with conventional LSC (Linear Slope Control) mode. Both DAC and EEPROM are controlled via a I^2C serial interface that operates by clock rates up to 1MHz.

The CN3969P incorporates with a UVLO reset circuit, power-down function, and exactly matched sense resistor. UVLO reset circuit ensure when supply power up, DAC output is to 0V until valid write-bit value takes place. It has a power down features that reduces the current consumption of the device to 1uA maximum.

The CN3969P is designed for auto focus and optical zoom camera phones, digital still cameras, and camcorders applications. The I^2C address for Driver IC is 0x18/0x1C when ID pin is high/low respectively, while the I^2C address for EEPROM is 0xB0/0xA0 when ID pin is high/low respectively.
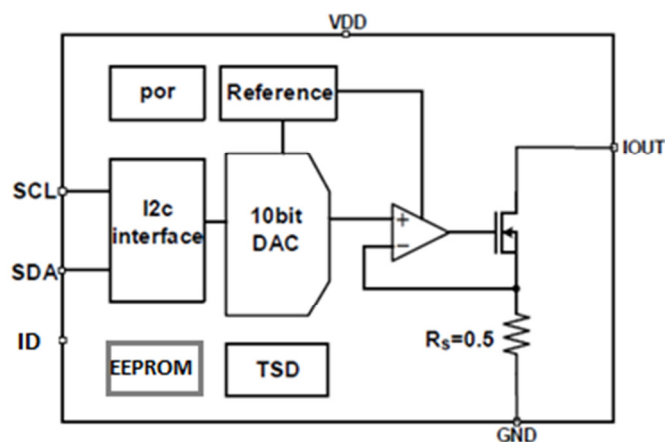
Features

- WLCSP package for minimum footprint
- Dual I^2C address selectable through ID pin
  - 0x18/0x1C when ID=high/low
  - 0xB0/0xA0 when ID=high/low
- SAC (Smart Actuator Control) mode
- 10-bit D-to-A converter
  - 9.5 bit Accuracy
  - 10bit resolution
- 10 KByte EEPROM
  - 64 byte per page
  - Partial Software Write Protest (PSWP)
- Current sinking of 120mA
- 117μA Iout resolution
- Fast I^2C serial interface (1.8V input available)
- Low current sleep mode
- 2.3 to 3.6 V power supply

Applications

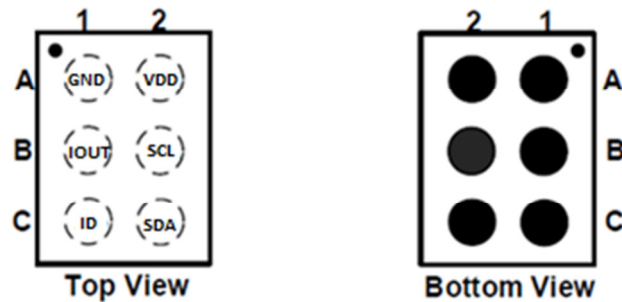- Digital camera
- Cell phone
- Lens auto focus

Package

- 6-Bump Chip Scale Package
- 0.76mm(W) x1.17mm(H) x 0.28mm(T)
- 0.4mm Bump Pitch

Block Diagram

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1. Pin Information

◆ Pin Assignments

Top View   Bottom View

◆ Pin Description

Pin Name	Pin Number	Description
GND	A1	Ground
VDD	A2	Power Supply
IOUT	B1	Output current Sink
SCL	B2	I2C data
ID	C1	VCM and EEPROM I2C Address Control
SDA	C2	I2C clock

2. Ordering Information

Order Part Number	Top Marking	Pb-Free	T_A	Package	
CN3969P	69P	Yes	-40 to +85°C	WLCSP6	Tape Reel,3K

3. Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Rating" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maxim rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Min.	Max.	Unit
VDD	Supply Voltage Range		4.5	V
Vin	Logic Input Voltage Range	-0.3	Vdd+0.3	V

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				Min	Max	Unit
T$_J$	Junction Temperature				150	°C
T$_S$	Storage Temperature Range		-40		150	°C
	Operating Temperature Range		-40		85	°C
ESD rating	Human Body Model (HBM)			8		KV

4. Recommend Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V$_{DD}$	Supply Input Voltage	2.3	2.8	3.6	V
Vin	Control Input Voltage	0		VDD	V
SCL	I2C Bus Clock Rate		400	1000	KHz
	Junction Temperature Range	-40		125	V
	Ambient Temperature Range	-40		85	°C

The Recommended Operating Conditions table defines the conditions for actual device operation to ensure optimal performance to the datasheet specifications. CHIPNEXT does not recommend exceeding them or designing to Absolute Maximum Ratings.

5. Electrical Characteristics

T$_A$ = 25°C, VDD =2.8V, V$_{IN}$=1.8V (unless otherwise specified)

Characteristics	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max	Units
Operation current						
Supply Voltage	V$_{DD}$	Linear mode	2.3	2.8	3.6	V
	I$_Q$	Quiescent mode(DAC=0)		0.34		mA
	I$_{ACT}$	Operation mode (DAC $\neq$ 0)			1	mA
Supply Current	I$_{SD}$	Shutdown mode(XSD=0)	-1		1	uA
	I$_{PD}$	Power down mode(PD=1)	-1		1	uA
Wait time	t$_{OPR}$	After VDD rising	1			ms
Logic Input/Output(XSD)						
Input current			-1		1	uA
Low level input voltage	V$_{IL}$	VDD=2.8V			0.54	V
High level input voltage	V$_{IH}$	VDD=2.8V	0.8			V
D/A						
Resolution (1)		Target=117uA/LSB		10		bit
Relative Accuracy (1) (2)	INL	Code from 1 to 1023	-4		+4	LSB

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Differential Nonlinearity (1) (2)	DNL	Guaranteed Monotonic	-1		+1	LSB
Max output current	Imax	Code=1023	116	120	124	mA
Output Driver						
Output Rdson	Rds	Rsense+Rsink, Iout=100mA, VDD=3V		2.0		Ω
Output Current @ PD			-1		1	uA
Over Temperature Protection						
Over Temp Protection	OTP_th			135		℃
Over Temp Protection Hysteresis	OTP_hys			10		℃
UVLO (Under Voltage Lockout)						
UVLO VDD threshold	Vth_uvlo	Iout<1uA, when VDD decrease to Vth_uvlo		2.0		V
UVLO hysteresis	Vhys_uvlo			100		mV
Logic Input and Output (SCL,SDA)						
Input Current			-1		1	uA
Low level Input Voltage	V_{IL}				0.54	V
High level Input Voltage	V_{IH}		0.8			V
SDA low level Input Voltage (open drain)	V_{IH}	Sink current =3mA			0.4	V
Glitch rejection			50			ns

(1) These are guaranteed by design spec

(2) Linearity is guaranteed for code 32 through code 992

14. Typical Application Circuit
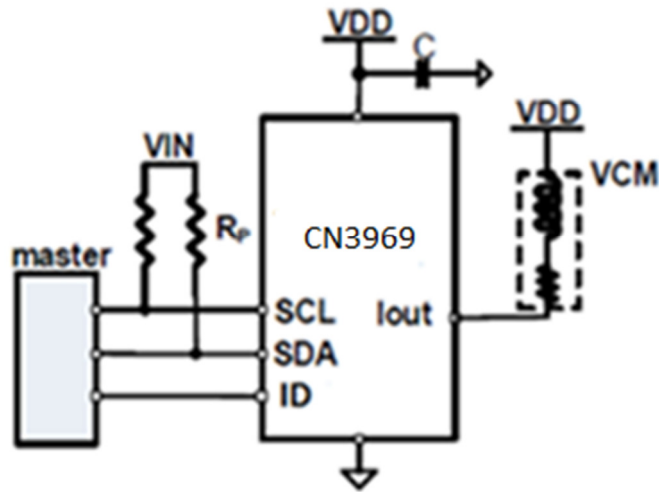
Figure 20. Typical Application Circuit

※ Power supply decoupling capacitor (C) should be placed as close to the VDD and VSS as possible.

※ The value of C is recommended more than 1uF.

※ PCB pattern of VDD, GND, OUTP and OUTN should be as short and wide as possible.

15. WLCSP-6 Package of Outline (All Units of Measure = mm)

0.760±0.02

A

PIN 1
Identifier

1.170±0.02

Top View

0.180±0.005

0.400±0.005

0.185±0.005

Bottom View

0.200±0.025

0.200±0.010

0.400±0.005

0.025±0.010

0.055±0.010

0.280±0.040